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ToucHMore

Company: Akhela
Speaker: Luigi Nuzzi – IoT Software Development Unit

General Information

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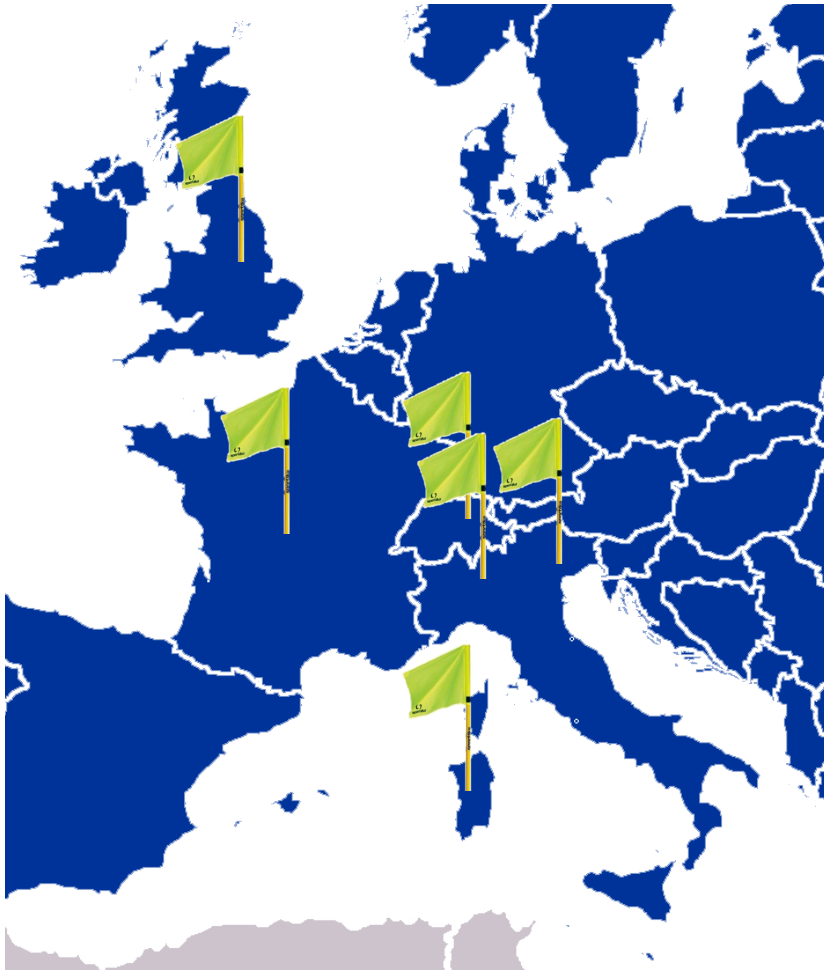

- Coordinator: Prof. Andrea Acquaviva (Polytechnic of Turin)
- Partners:
  - POLITECNICO DI TORINO Italy
  - UNIVERSITA DEGLI STUDI DI VERONA Italy
  - ATEGO United Kingdom & France
  - CEA France (Commissariat à l'énergie atomique et aux énergies alternatives)
  - CSEM Switzerland (Centre Suisse d'Electronique et de Microtechnique)
  - AKHELA SRL Italy (AKH)
  - UNIVERSITY OF YORK United Kingdom (UY)
- Type of project: FP7 Collaborative Projects
- Budget Total: 3970 K€

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WP Organization

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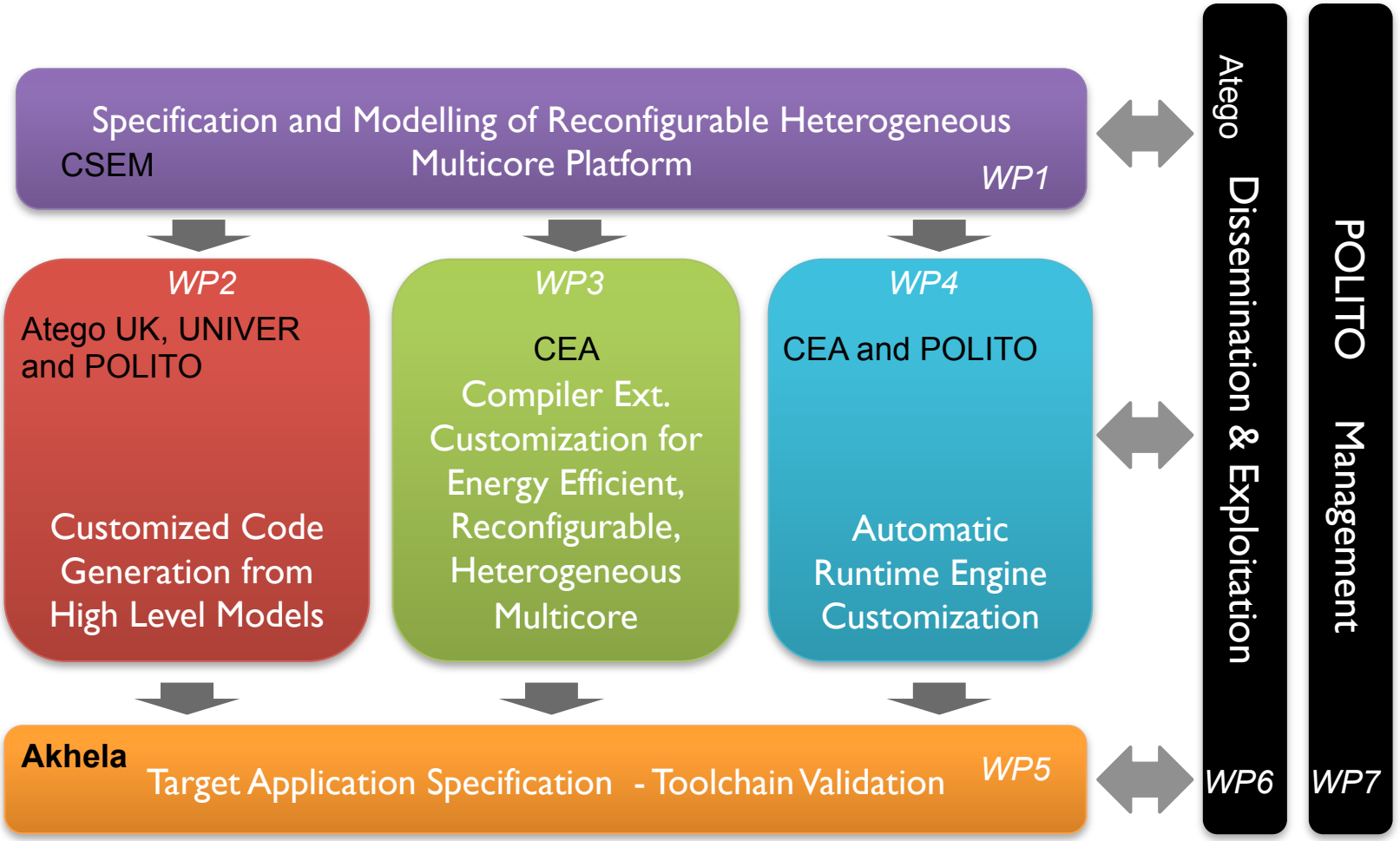

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Project Themes

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- More Functionalities
- Cost Saving
- Time To Market
- Energy Saving
- More Speed
- Faster Prototyping
- Focus on Application rather then on Infrastructure

EMBEDDED

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Project Motivations

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*Recent trends in **embedded system** architectures brought a rapid **shift** towards **multicore, heterogeneous** and **reconfigurable platforms**.*

*This makes **chip design** enormously **complex** and imposes a large **effort for the programmers** to develop their applications. For this reason, new and more **efficient tools for software development are needed** to ensure software **productivity** and **time to market** of new applications.*

*The **automation of the software design** process starting from high level models all-the-way down to a customized and implementation on specific architectures **is a key factor to increase programmer productivity**.*

From TOUCHMORE Website

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TouCHMore Concept

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Why Multicores for Energy & Speed?

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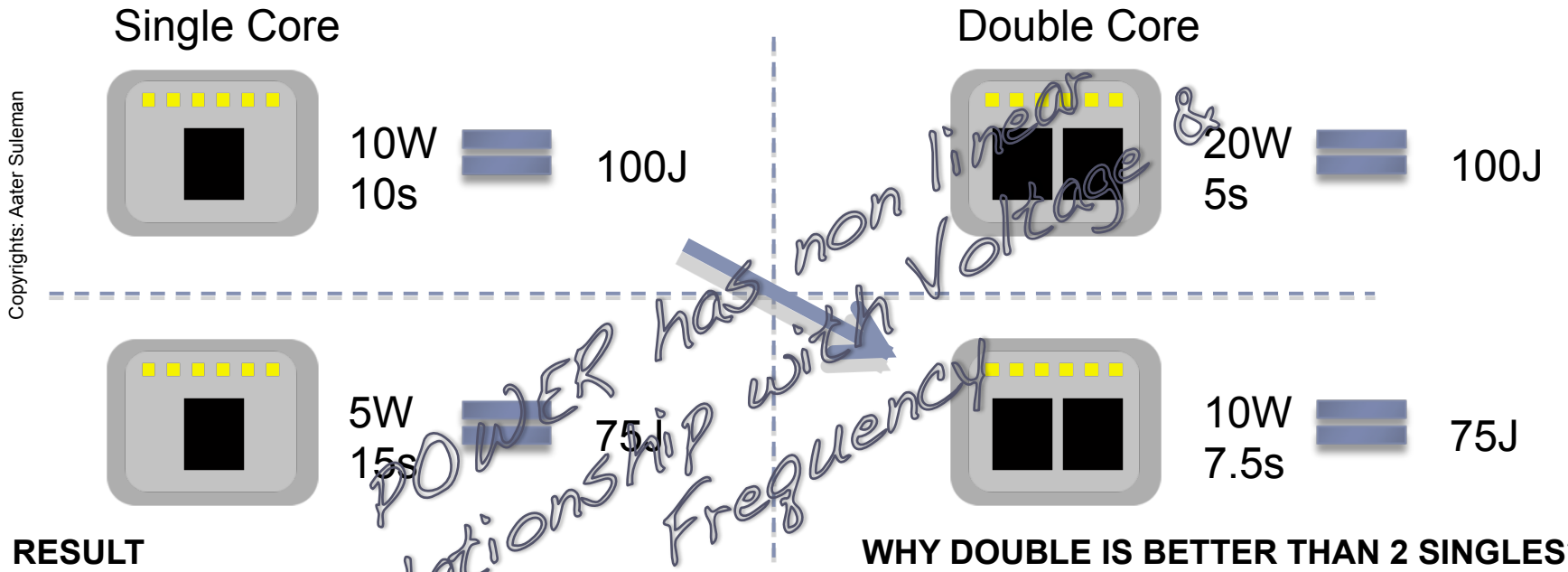

RESULT

Multicore by itself doesn't guarantee Energy saving & Speed, it always depends on:

1. Each Core efficiency
2. Programmer experience

SOLUTION

Intelligent Tool-Chains will become a MUST

WHY DOUBLE IS BETTER THAN 2 SINGLES?

1. 2 Singles require wiring (EMI+Dissipation)
2. Speed will be affected

WHY SLOW IS BETTER THAN FAST?

FAST cores use prediction. If prediction is wrong some Energy is wasted.

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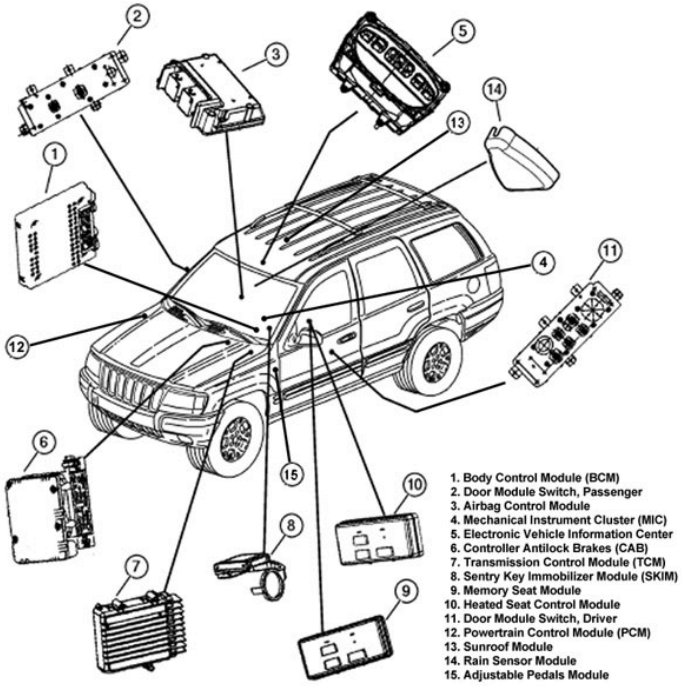
Why Automotive for Explotation?

http://www.wjjeeps.com/ecm_02.jpg



The Automotive Industry need to reduce #of ECU to:
Save Costs
Reduce Power Consumption
Reduce EMC problems
Reduce Wiring…

…While integrating more Features, which means:
More Speed and
computational power.

Car Infotaiment Evolution

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Consumer world:
Data Storage, Portable, Connectivity

50s 60s 70s 80s 90s 00s 10s

Zenith Royal-T (1953)

Integ' d Power Amp

Integ' d Signal Proc IC

Integ' d RF FE

Digital AM/FM

Digital Broadcast

Multi-Standards

Data Services

SW Complexity

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Tool Flow – Overview

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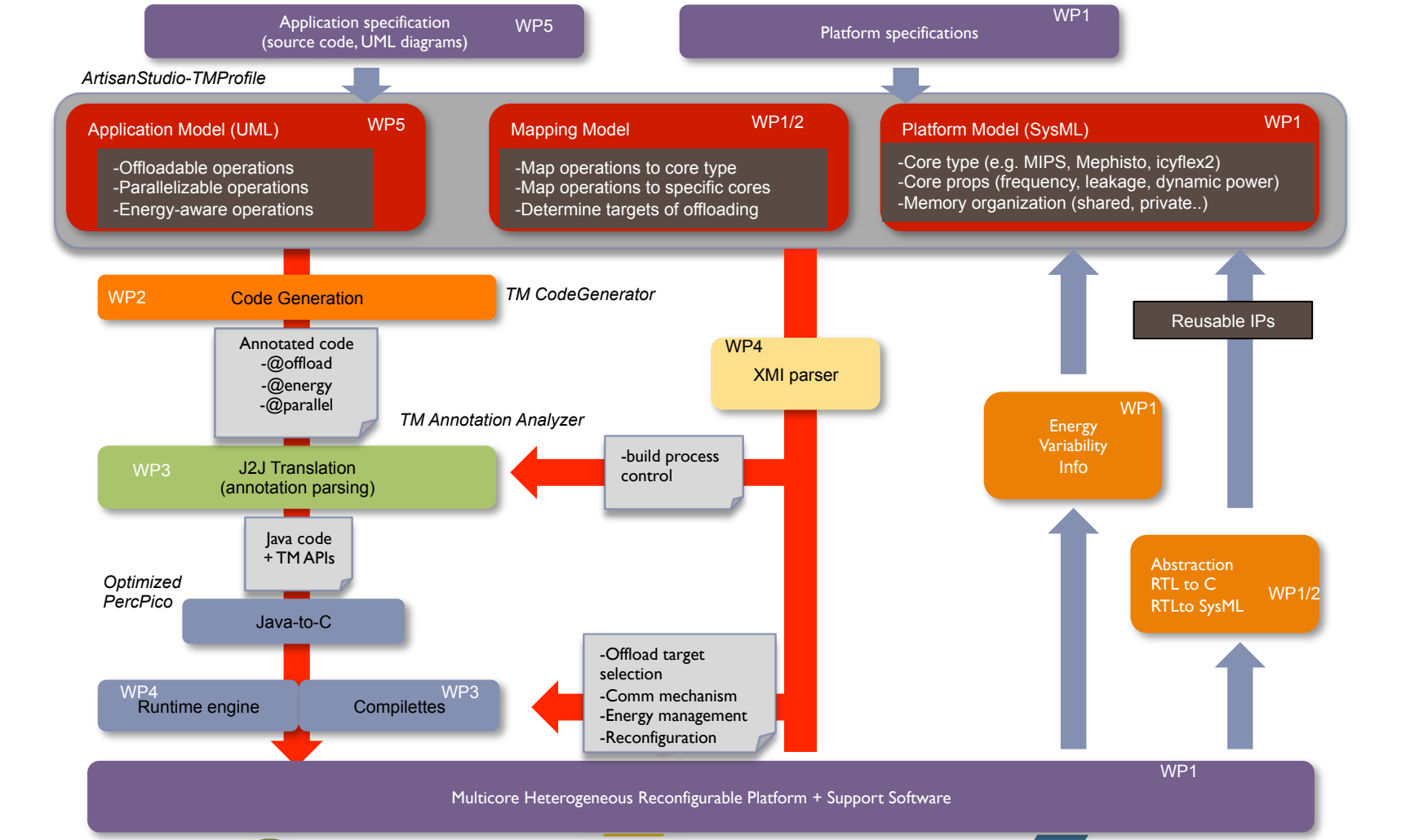

Artisan Application Model

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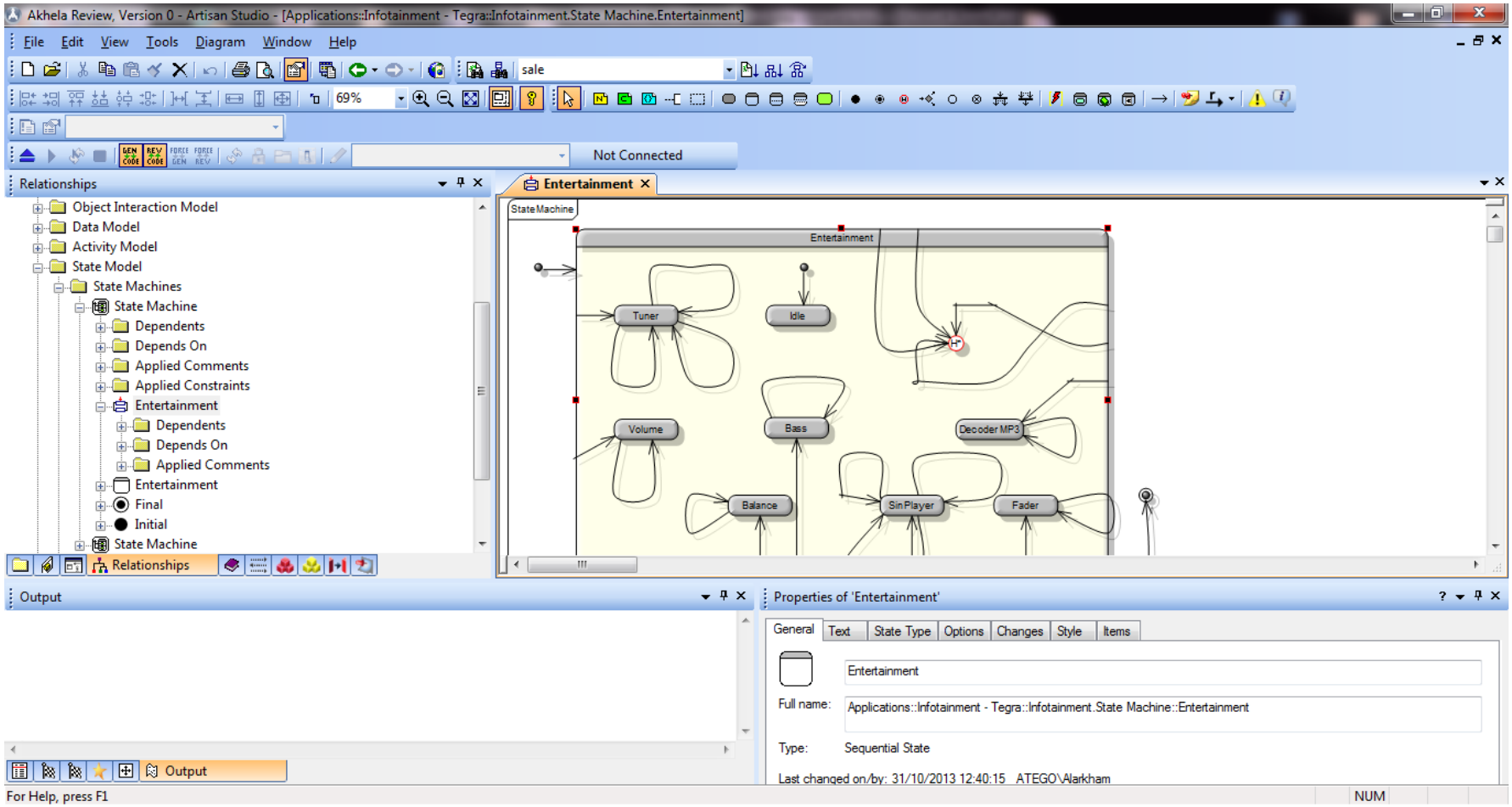
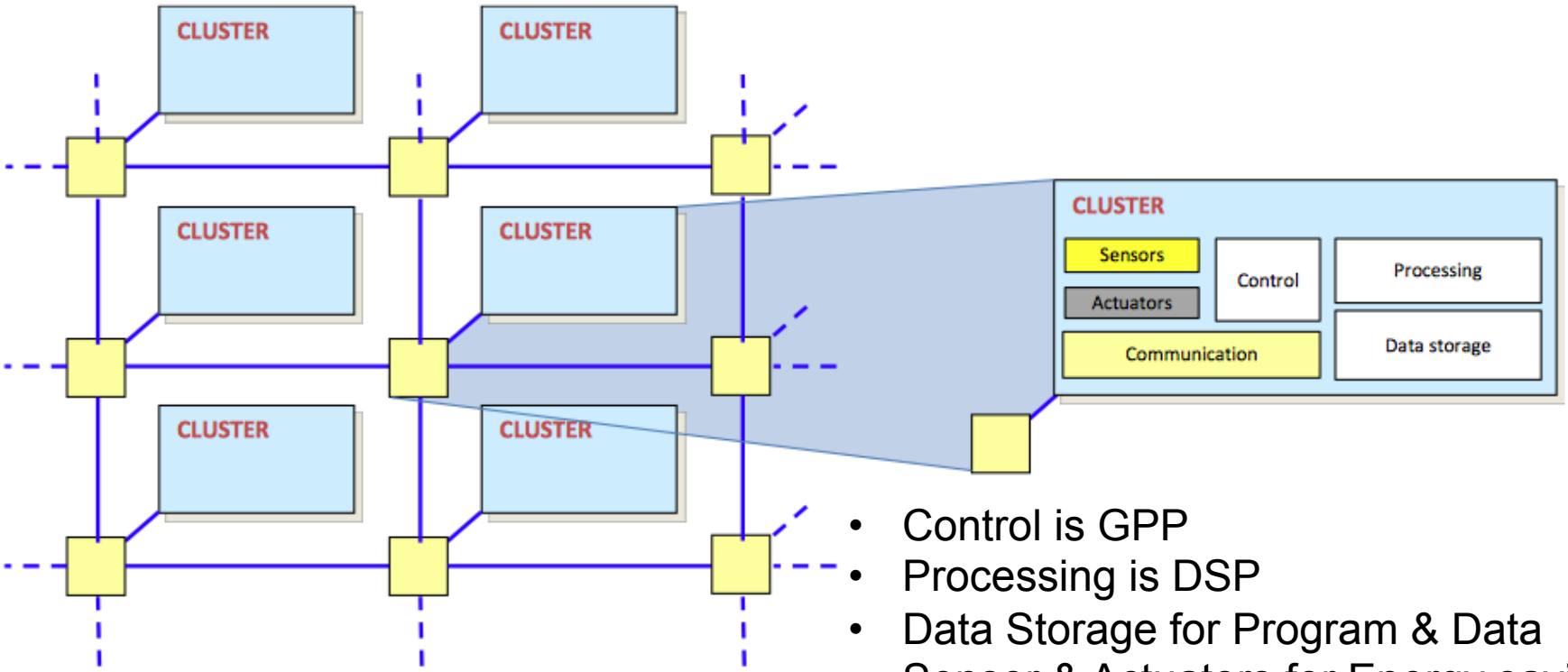
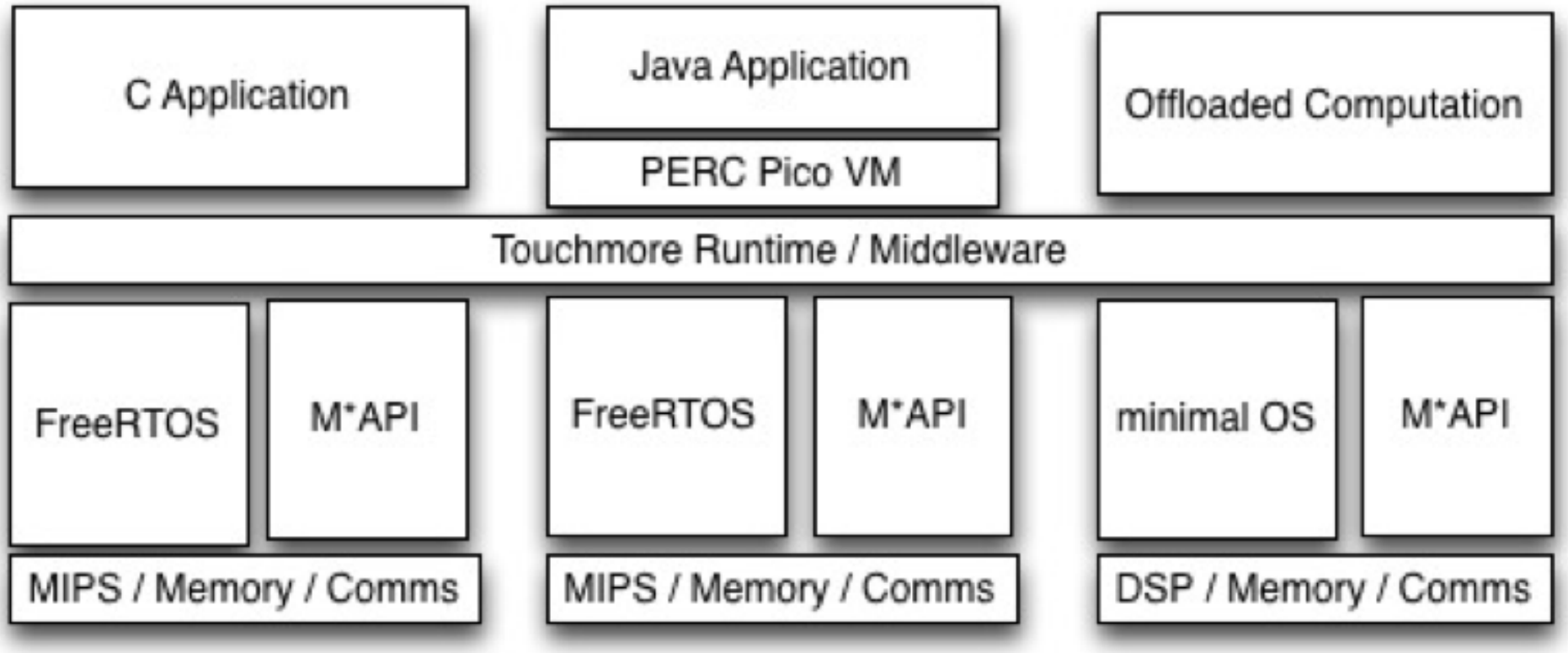


The GENEPY Platform



- Control is GPP
- Processing is DSP
- Data Storage for Program & Data
- Sensor & Actuators for Energy saving
- Communication Interface

Software Platform



GENEPY SoC (CSEM & CEA)

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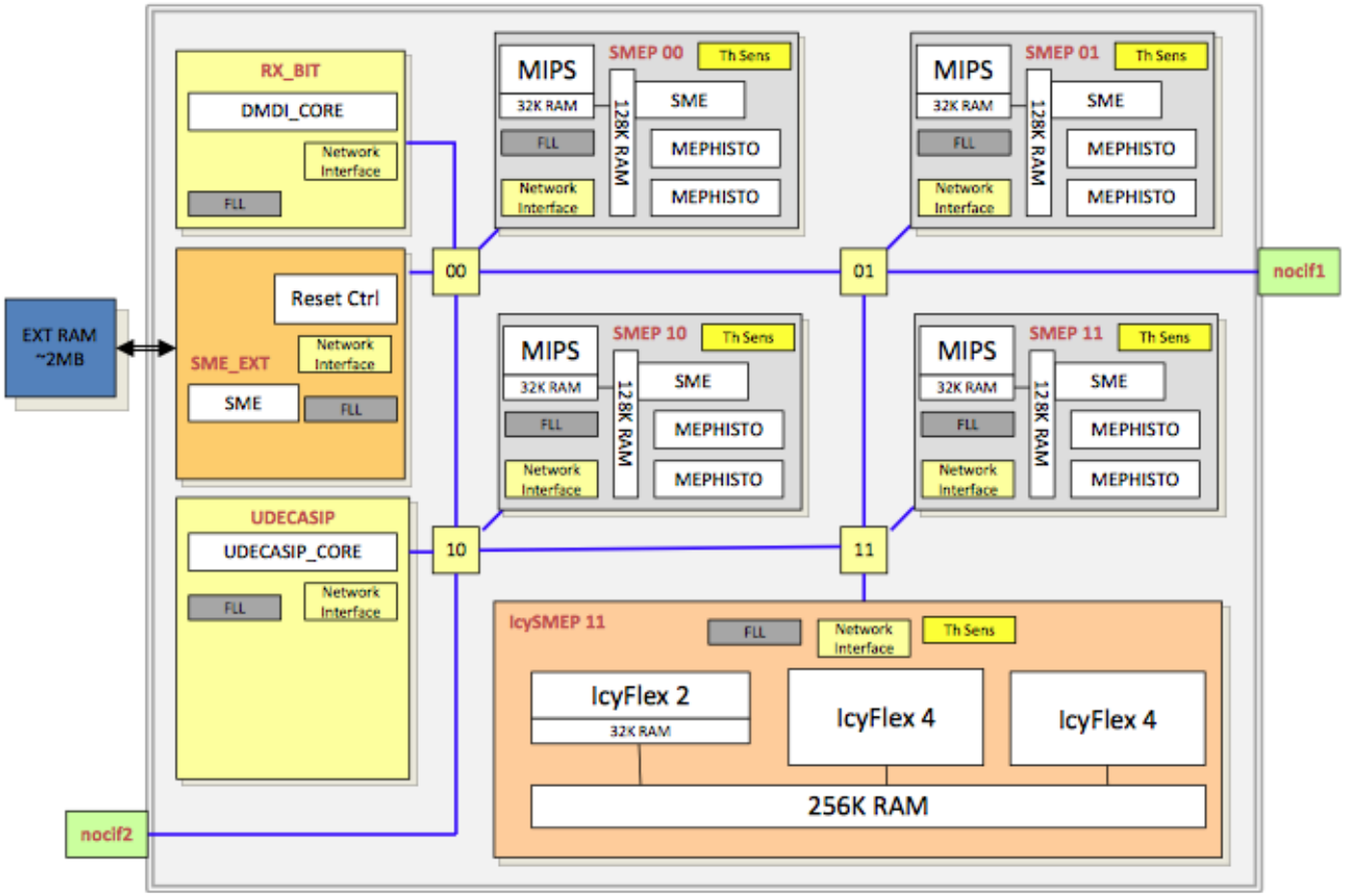
30mm2 in technology CMOS 65nm



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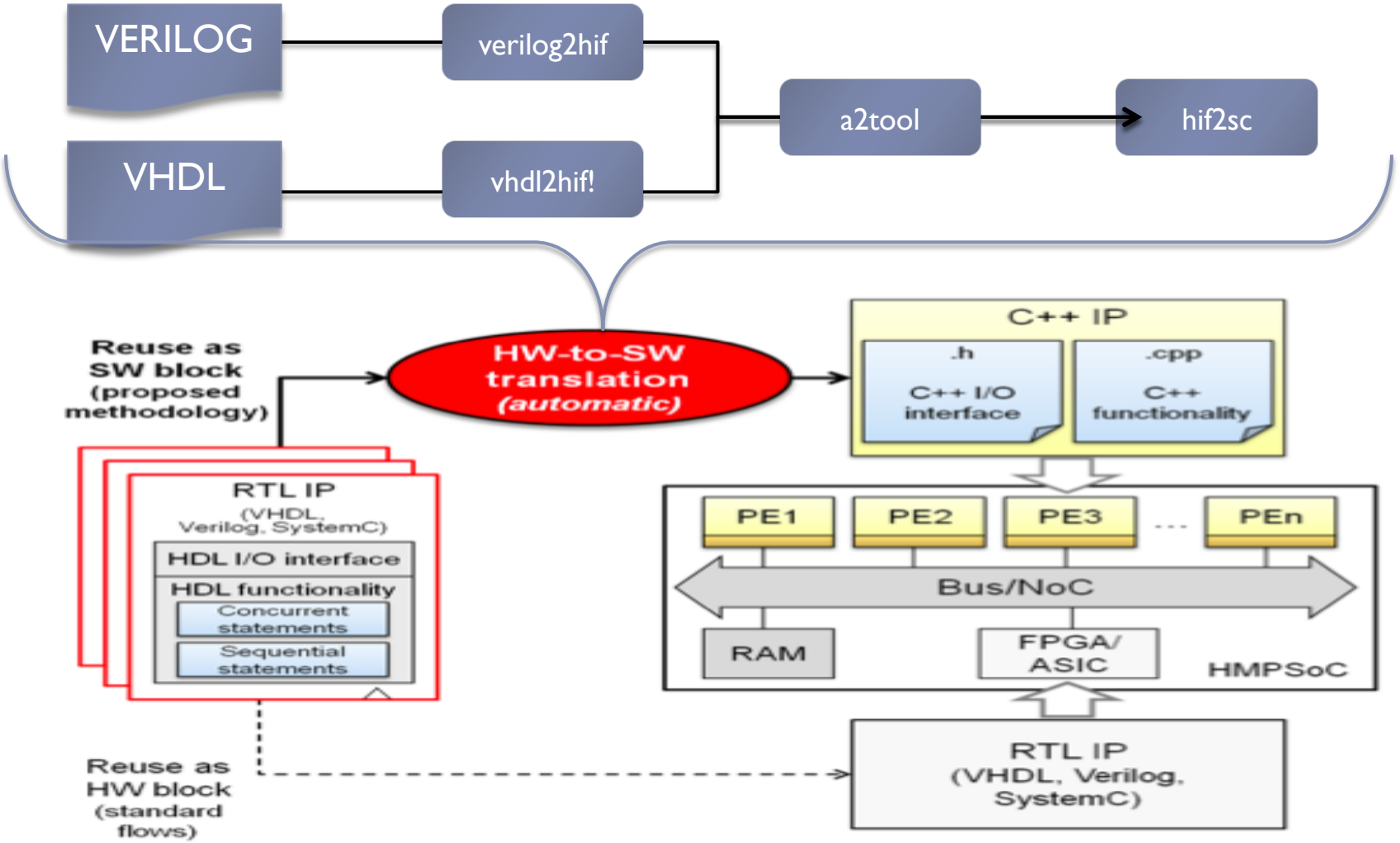
The RTL2C++ Proposal



Results

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	C++ IP	Manual code				H2C++ code					
		C++ loc	Assembly loc	main_IP() invoc.	Sim. time(s)	C++ loc	Assembly loc	Main_IP() invoc.	C++ scheduler invoc.(s)	Sim. Time w.out abstract types(s)	Sim. Time with abstract types(s)
I	ROOT	18	79	100,000	0.26	223	985	100,000	7,200,004	0.92	0.37
	GCD	25	45	100,000	1.58	114	186	100,001	700,101	10.38	1.77
	ECC	224	1,538	100,000	0.31	390	1,724	200,001	200,259	0.65	0.34
II	ADPCM	271	318	100,000	3.96	284	749	738,000	738,000	58.81	4.30
	FFT	876	2,731	100,000	0.41	3,643	8,858	210,000	2,731,000	1.83	1.28
	DSPI	353	721	100,000	2.13	2,891	3,112	200,000	1,605,020	9.12	3.87
III	DIST	37	203	100,000	1.46	116	247	100,065	800,520	13.13	1.70
	DIV	22	34	100,000	1.45	67	74	200,001	1,000,001	12.72	1.55
	CRC	235	714	100,000	3.49	1,621	5,275	1,520,000	100,000	13.52	5.36

- ROOT: Square root device (VHDL).
- GCD: Greatest common divisor (VHDL).
- ECC: Error Correction Code (VHDL).
- ADPCM: Adaptive Differential Pulse Code Modulation (SystemC).
- FFT: Fast Fourier Transform (VHDL).
- DSPI: Synchronous Peripheral Interface (Verilog).
- DIST: Pixel Distance Encoder (VHDL).
- DIV: Filter for RGBA representation of pixels (VHDL).
- CRC: Cyclic-Redundancy Checking (VHDL).

I = complete C++ implementation available
II = Partial equivalent C++ implementation.
III = Manually implemented from scratch (DIST, DIV, CRC).

NOTE:
The synthesis of the C++ code has been instantaneously accomplished by H2C++, while 28 person-days have been spent for implementing and verifying the equivalent C++ code by hand.

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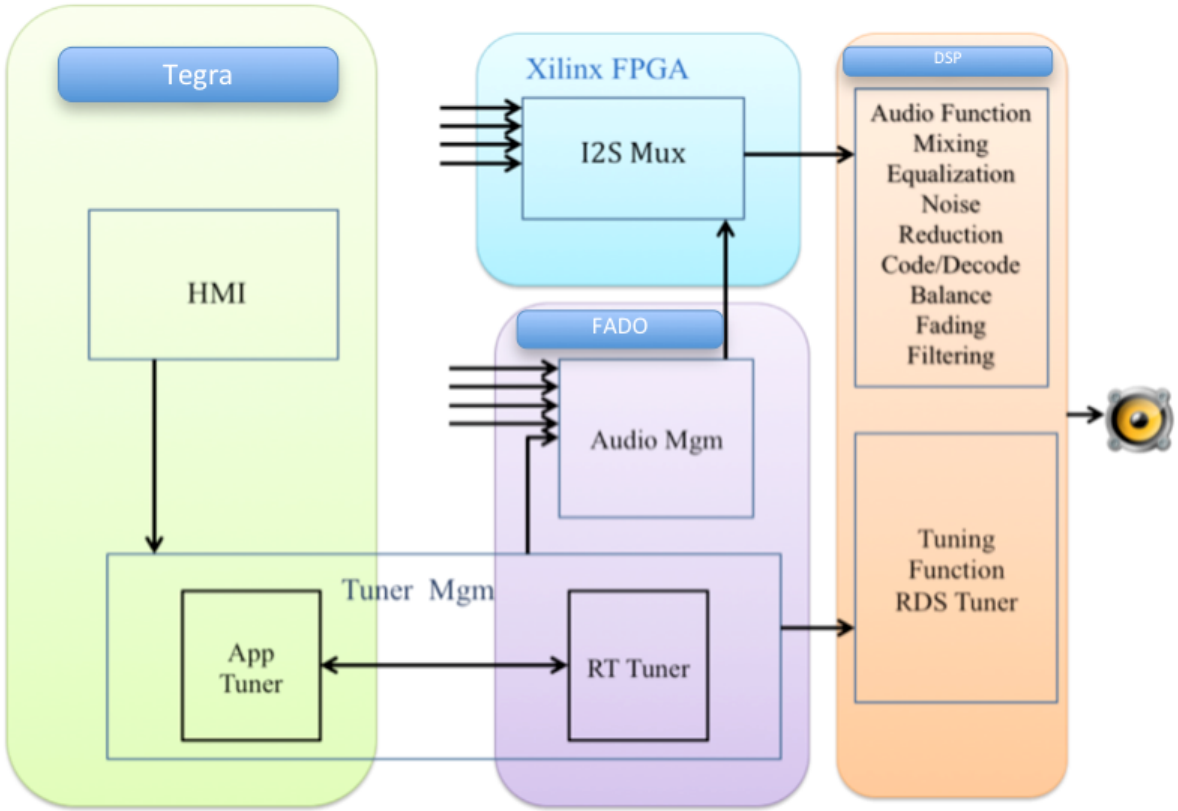
Infotainment Target Components



Main Outcome and Result

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- A complete automatic customizable tool-chain for multicore platform will be developed and evaluated on a complex heterogeneous next generation multicore chip designed by CEA and CSEM including clusters of general purpose processors as well as DSPs.
- The evaluation is obtained using automotive infotainment applications provided by AKHELA. Target application
- The generated code will be optimized for the selected platform considering energy-efficiency and robustness with respect to process variabilities.

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Exploitation Expectation

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- Consistent (20%) reduction of time to market and cost for the design of complex multicore systems
- Reduction in the cost of the system design by 15% through automation and customization of code generation
- Achievement of energy efficiency and robustness in next generation multicore platforms

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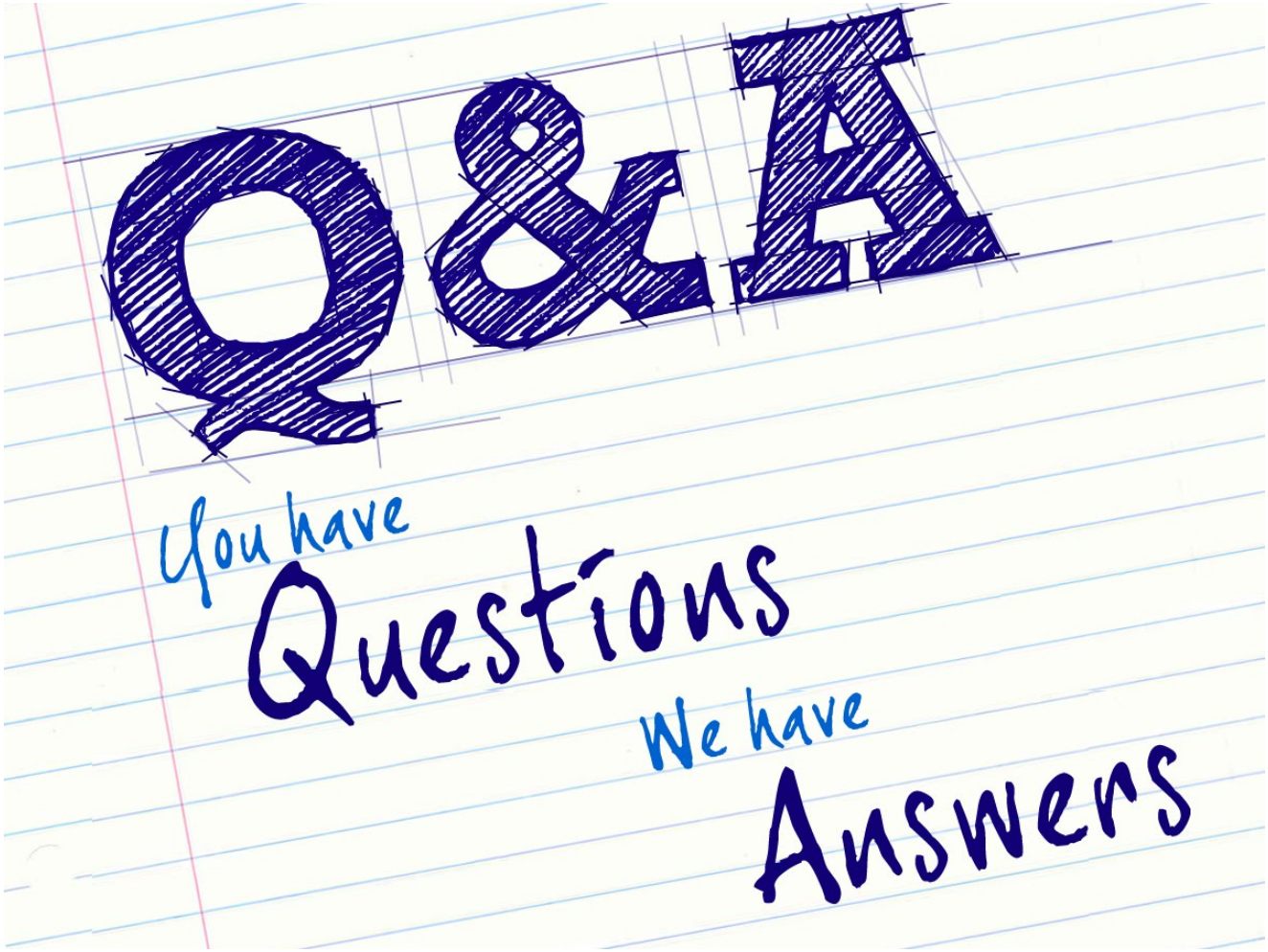

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